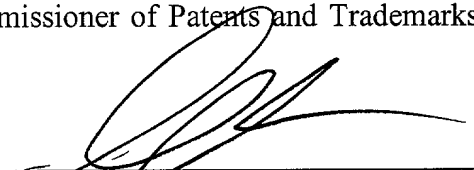


EXPRESS MAIL number EL811589576US

Deposited August 22, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, DC 20231


Shahan Islam

3246/FLK/DIV of 2798/FLK

IN THE UNITED STATES PATEN AND TRADEMARK OFFICE

-----X

Applicant: Nobuo MAMADA

Prior Application

Serial No.: 09/411,960

Filed: November 17, 1999

For: Ceramic Board Having Thereon
Coupled Ceramic Capacitors &
Method For The Manufacture
Thereof

Examiner: N. HA

Group Art Unit: 2831

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination, please amend the above identified application as follows:

IN THE SPECIFICATION:

Page 1, before line 3, please insert -- This is a divisional of U.S. Application

Serial No. 09/441,960, filed November 17, 1999 entitled Ceramic Board Having Thereon

Coupled Ceramic Capacitors & Method For The Manufacture Thereof--

Please replace the paragraph beginning at line 22 of page 3, with the following rewritten paragraph:

5 --the capacitors are disposed at substantially plane-symmetrical positions on two opposite surfaces of the circuit board and substantially identical voltages are applied to the capacitors,

 wherein the electronic circuit is of a type in which voltages applied to the capacitors have frequencies varying in an audible frequency band.--

10 Please delete the paragraphs beginning at line 26 of page 3 and ending at line 19 of page 4.

IN THE CLAIMS

Please delete the pending claims and insert therefore the following claims:

15 1. (New) A method for mounting multilayered ceramic capacitors on a circuit board having a front surface and a back surface, wherein each capacitor includes a body having dielectric layers formed of a dielectric ceramic material and internal electrode layers and a pair of external terminal electrodes formed on two sides of the body, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode
20 layers being connected in parallel to the external terminal electrodes in an alternate manner, the method comprising the steps of:

 forming lands at substantially plane-symmetrical positions on the front and the back surfaces, wherein every two lands disposed at their substantially plane-symmetrical positions are connected each other; and

25 mounting the capacitors on the lands of the front and the back surfaces and electrically coupling the external terminal electrodes of the capacitors to the lands on the front and the back surfaces.

2. (New) The method of claim 1, wherein said two lands are electrically coupled each other by a through hole formed therein.

5 3. (New) The method of claim 1, wherein the capacitors are substantially identical each other.

4. (New) The method of claim 1, wherein the capacitors are connected in parallel.

10 5. (New) The method of claim 1, wherein voltages applied to the capacitors are varied.

6. (New) The method of claim 1, wherein voltages applied to the capacitors have frequencies varying in an audible frequency band.

15 7. (New) A method for mounting multilayered ceramic capacitors on a circuit board having a front surface and a back surface, wherein each capacitor includes a body having dielectric layers formed of a dielectric ceramic material and internal electrode layers and a pair of external terminal electrodes formed on two sides of the body, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode layers being connected in parallel to the external terminal electrodes in an alternate manner, the method comprising the step of:

mounting the capacitors on substantially plane-symmetrical positions of the front and the back surfaces, respectively, wherein the capacitors are substantially identical each other and substantially identical voltages are applied to the capacitors.

25

8. (New) The method of claim 7, wherein said mounting step includes the steps of:
forming lands at substantially plane-symmetrical positions on the front and the back
surfaces, wherein every two lands disposed at their substantially plane-symmetrical positions
are connected each other; and

5 mounting the capacitors on the lands of the front and the back surfaces such that the
external terminal electrodes of the capacitors are electrically coupled to the lands on the front
and the back surfaces.

9. (New) The method of claim 8, wherein said two lands are electrically coupled each
10 other by a through hole formed therein.

10. (New) The method of claim 7, wherein the capacitors are substantially identical
each other.

11. (New) The method of claim 7, wherein the capacitors are connected in parallel.
15

12. (New) The method of claim 7, wherein voltages applied to the capacitors are varied.

13. (New) The method of claim 7, wherein voltages applied to the capacitors have
20 frequencies varying in an audible frequency band.

14. (New) A method for mounting multilayered ceramic capacitors on a circuit board
having a front and a back surfaces, the capacitors being used in an electronic circuit as
components thereof and voltages applied to the capacitors being varied, wherein each
25 capacitor includes a body having dielectric layers formed of a dielectric ceramic material and

internal electrode layers and a pair of external terminal electrodes formed on two sides of the body, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode layers being connected in parallel to the external terminal electrodes in an alternate manner, the method comprising the steps of:

5 forming lands at substantially plane-symmetrical positions on the front and the back surfaces, wherein every two lands disposed at their substantially plane-symmetrical positions are connected each other; and

 mounting the capacitors on the lands of the front and the back surfaces such that the capacitors are disposed at substantially plane-symmetrical positions and the external
10 terminal electrodes of the capacitors are electrically coupled to the lands on the front and the back surfaces, wherein the capacitors are substantially identical each other and substantially identical voltages are applied to the capacitors.

15 15. (New) The method of claim 14, wherein said two lands are electrically coupled each other by a through hole formed therein.

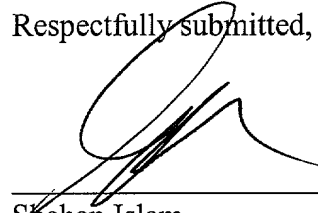
16. (New) The method of claim 14, wherein the capacitors are substantially identical each other.

20 17. (New) The method of claim 14, wherein the capacitors are connected in parallel.

18. (New) The method of claim 14, wherein voltages applied to the capacitors are varied.

25 19. (New) The method of claim 14, wherein voltages applied to the capacitors have frequencies varying in an audible frequency band.

Respectfully submitted,



Shahan Islam,
Registration No. 32,507

5

10 Date: August 22, 2001
Rosenman & Colin LLP
575 Madison Avenue
New York, NY 10022-2585
(212) 940-8564

FOR FILING

APPENDIX A - VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

5 The paragraph beginning at line 22 of page 3 has been replaced with the following
rewritten paragraph:

 --the capacitors are disposed at substantially plane-symmetrical positions on two
opposite surfaces of the circuit board and substantially identical voltages are applied to the
10 capacitors,

 wherein the electronic circuit is of a type in which voltages applied to the capacitors
have frequencies varying in an audible frequency band.--

 Please delete the paragraphs beginning at line 26 of page 3 and ending at line 19 of
15 page 4.